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EXAMINER	
CEHIC, KENAN	
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2416	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,914	CHEE ET AL.	
	Examiner	Art Unit	
	KENAN CEHIC	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claim 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freeman (US 4,862,399) and English, ADA 95: The Craft of Object-Oriented Programming, "Glossary".

For claim 2, Freeman discloses a method for use in verification of a device (and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit") comprising:

providing a plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns

to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

providing indications (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found") which may be of a first or second state (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found"; checkmarks for each pattern; see col 9 lines 35 through col 10 line 40 "pattern is not needed…only those patter) , for each of the plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests"); generating a packet (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test

vectors…Pattern PC…test patterns….all block level tests"); if the indication of the packet class of the generated packet is in the first state (see fig. 4, "Already detected"; "This pattern", "Detected Inclusive", checksmarks for the patterns; see col 9 lines 35 through col 10 line 40 "two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…") testing the device (see fig 2; Small, Nonredundant Chip-level testset and col 9 line 35 through col 10 line 40 "pattern is noted…those patterns…are kept…until the test pattern Pc contain...results in a efficient testset which exhaustively test the chip in a practical way" And col 11 lines 1-50 " and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit")

if the indication of the packet class of the generated packet is in the first state (see fig. 4; "Already detected"; "This pattern", "Detected Inclusive", checksmarks for the patterns; see col 9 lines 35 through col 10 line 40 "two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…"), noting/making/changing an indication for the packet class (see fig 4; "This pattern", "Detected Inclusive" and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found"; col 9

line 35 through col 10 line 40 “pattern is noted if it detects a new fault…those patterns that may be useful in detecting a fault are kept….test is added to the list”)

For claim 3, A method for use in verification of a device (and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit") comprising:

providing a plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; col 9 lines 40 through col 10 line 40 “ test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests”);

providing a indications (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found” and Retain Chip-Level Test…update…List…already found”), which may be of a first or a second state (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found” and Retain Chip-Level Test…update…List…already found”; checkmarks for each pattern; see col 9 lines 35 through col 10 line 40 “pattern is not needed…only those patter), for each of the plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 “ test patterns…produces the necessary test

patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

generating a packet (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests"); if the indication of the packet class of the generated packet is in the first state (see fig. 4, "Already detected"; "This pattern", "Detected Inclusive", checksmarks for the patterns; see col 9 lines 35 through col 10 line 40 "two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…") testing the device (see fig 2; Small, Nonredundant Chip-level testset and col 9 line 35 through col 10 line 40 "pattern is noted…those patterns…are kept…until the test pattern Pc contain...results in a efficient testset which exhaustively test the chip in a practical way" And col 11 lines 1-50 " and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and

retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit");if the indication of the packet class of the generated packet is in the second state (see fig. 4, “Already detected”; “This pattern”, "Detected Inclusive", checksmarks for the patterns; see col 9 lines 35 through col 10 line 40 “two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…”), not testing the device (see fig 2; retain chip-level test, "small, nonredundant chip-level testset”; col 9 lines 40 through col 10 line 40 “remaining patterns of no interest are discarded…tests is discarded…additional pattern PC’’ is redundant and can be discarded…” col 12 lines 57 through col 13 line 43 " discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit")

For claim 4, Freeman discloses A method for use in verification of a device (and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit") comprising: providing a plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; col 9 lines 40 through col 10 line 40 “ test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk...Pk represents a fault test

pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

providing an indication (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found"), which may be of a first or a second state (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found"; checkmarks for each pattern; see col 9 lines 35 through col 10 line 40 "pattern is not needed…only those patter), for each of the plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

generating a packet (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

if the indication of the packet class of the generated packet is in the second state (see fig. 4, “Already detected”; “This pattern”, "Detected Inclusive", checksmarks for the patterns; see col 9 lines 35 through col 10 line 40 “two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…”), not testing the device (see fig 2; retain chip-level test, "small, nonredundant chip-level testset”; col 9 lines 40 through col 10 line 40 “remaining patterns of no interest are discarded…tests is discarded…additional pattern PC’’ is redundant and can be discarded…” col 12 lines 57 through col 13 line 43 " discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit")

For claim 5, Freeman discloses A method for use in verification of a device (and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit") comprising:

(a) providing a plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; col 9 lines 40 through col 10 line 40 “ test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests”);

(b) providing an indication (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found"), which may be of a first or a second state (see fig 4; Already detected, detected inclusive and fig 2; List of Test…already found" and Retain Chip-Level Test…update…List…already found"; checkmarks for each pattern; see col 9 lines 35 through col 10 line 40 "pattern is not needed…only those patter), for each of the plurality of packet classes (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

(c) generating a packet (see fig 2; Large, Redundant Chip-level Testset; see fig 4; Testset, Fault; col 9 lines 40 through col 10 line 40 " test patterns…produces the necessary test patterns to be applied…to block under test…test patterns applied …all of the test patterns… ..obtain a test pattern…..TESTSET represents a list of all patterns P1-Pk..faults column lists all the patterns Pk to be selected...Pk represents a fault test pattern...tests are determined….sets of chip-level test vectors…Pattern PC…test patterns….all block level tests");

(d) if the indication of the packet class of the generated packet is in the second state (see fig. 4, "Already detected"; "This pattern", "Detected Inclusive", checksmarks for the

patterns; see col 9 lines 35 through col 10 line 40 “two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…”), not testing the device (see fig 2; retain chip-level test, "small, nonredundant chip-level testset”; col 9 lines 40 through col 10 line 40 “remaining patterns of no interest are discarded…tests is discarded…additional pattern PC’’ is redundant and can be discarded…” col 12 lines 57 through col 13 line 43 " discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit")

;(e) if the indication of the packet class of the generated packet is in the first state (see fig. 4; “Already detected”; “This pattern”, "Detected Inclusive", checksmarks for the patterns; see col 9 lines 35 through col 10 line 40 “two sets of chip level test vectors yield the same test at the block-level…tests is discarded….only one…is retained...Pattern Pc is then compared to all other chip level test pattern…”), testing the device (see fig 2; Small, Nonredundant Chip-level testset and col 9 line 35 through col 10 line 40 "pattern is noted…those patterns…are kept…until the test pattern Pc contain...results in a efficient testset which exhaustively test the chip in a practical way” And col 11 lines 1-50 " and col 12 lines 57 through col 13 line 43 "method of determining...output test pattern is reliably reproduced from a set of test input pattern....digital circuit…screening said simulated…input patterns to one antoher and retaining only those…pattern which applies…discarding those digital circuit input patterns…applying said compared ….patterns to an actual manufactured digital circuit")

noting/making/changing an indication for the packet class of the generated packet (see fig

4; “This pattern”, "Detected Inclusive" and fig 2; List of Test…already found” and Retain Chip-Level Test…update…List…already found”; col 9 line 35 through col 10 line 40 “pattern is noted if it detects a new fault…those patterns that may be useful in detecting a fault are kept….test is added to the list”)

For claim 6, Freeman discloses further comprising repeating steps (c) through (e) thereof (see col 9 line 25 through col 10 line 40 “all block level test are determined….test is added to the list …screened…procedure is repeated”).

While Freeman discloses indicators for a packet class (see fig 4), Freeman fails to explicitly disclose:

For claim 2 and 3, flag, having two states, as indicators, and changing the state of a flag.

For claim 5, injection flag, having two states, as indicators, and changing the state of a injection flag.

English from the same or similar field of endeavor discloses:

For claim 2 and 3, flag, having two states, as indicators, and changing the state of a flag (see page 5; “Flag”: A Boolean value which can be “set” to True or ‘reset’ to False”).

For claim 5, injection flag, having two states, as indicators, and changing the state of a injection flag (see page 5; “Flag”: A Boolean value which can be “set” to True or ‘reset’ to False”).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Freeman by using the features, as taught by English, in order to provide an means / programming technique (using flags) which indicates a certain state of a program/variables with minimal storage (memory) use. Through the use

of flags a system/program (like the one of Freeman) can use known flags to indicate a certain property/state of either the program/ variable with minimal memory and processing resources.

Furthermore, each of the claimed elements was known in the art, and a person of ordinary skill in the art could have combined the use of flags into the program/method of Freeman each element would have preformed the same function as it did seperately. The use of flags in the Freeman system would not change the operation of the Freeman system, as the use of flags is merely using variables in a program that indicate a certain state and one of ordinary skill would have recognized that the results of the combination would have been predictable.

Response to Arguments

2. Applicant's arguments filed 10/14/2008 have been fully considered but they are not persuasive.

For claim 2, the applicant argues, on page 4 of the remarks, that the motivation and reasoning for combining the teachings of Freeman and "Glossary" (hereinafter D1) are improper. The applicant specifically points out that Freeman finds redundant patterns and discards them, further concluding that less storage is used than "the present flag use, wherein data packets are retained with an accompanying set flag rather than discarded". It appears that in the quoted section the applicant is arguing that those features are not disclosed in the combination of Freeman and D1. If this is the case, it is pointed out that such limitations are not recited in claim 2. Claim 2 does include limitations where

packets are retained and not discarded. Claim 2 does not exclude such a feature / possibility. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the present flag use, wherein data packets are retained with an accompanying set flag rather than discarded") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Regarding the arguments presented questioning the combination and rational of the combination, the applicant argues that the combination would not result in less storage/memory or processing resources. As pointed out in the quoted sections and figures 2 and 4, it is clear that Freeman discloses keeping track of which patterns are useful. This is clearly described in figure 2 ("List of Tests At Block-Level already found", "Retain CHIP-LEVEL TEST and UPDATE LIST…"); Figure 4 ("ALREADY DETECTED", "DETECTED INCLUSIVE"), col 10 line 1-10 "A pattern is noted…those patterns that may be useful….are kept". It is clear from those figures and their description that Freeman's teaching discloses associating an indicator (for example using a checkmark (which can be considered as a variable/ or any type of digital signal) in a table as shown in Figure 4) for patterns / testcases which are useful and also which have already been tested. The possibility that such pattern or testcase is later discarded is moot, since some type of indication/variable is present and associated with a pattern or testcase. Furthermore, claim 2 does not exclude such a possibility/feature of discarding. Thus it would have been obvious to use a flag (ie a Boolean value) for indicators (such as the

checkmarks in figure 4) which are associated with a pattern/testcase. Such a simple and well known variable can be effectively used to convey the status (such as the checkmarks in figure 4) associated with patterns / test cases. Using such a Boolean value (ie a bit) would minimize memory / processing resources needed to execute the teachings of Freeman. A combination/modification using a flag (as taught by D1) would not change the principle of operation of Freeman and is even suggested / implied by the use of checkmarks in figure 4 of Freeman. It would have been obvious to a person of ordinary skill in the art to use the well-known method of a Boolean value (flag) to keep track / indications associated with patterns / testcases as disclosed by Freeman. For the above reasons, the examiner fails to see that the combination of Freeman and D1 do not disclose the limitations of claim 2 and that the combination is improper.

Lastly, the applicant argues, on page 5 of the Remarks, applicant argues that whether testing is done based on a flag is not disclosed by the combination of Freeman and D1. Specifically, applicant points out that the whether testing is done based on the discarding of patterns. Freeman discloses using indicators associated with pattern / testcases to find new / useful / redundant patterns or testcases, as described above. Based on a indicator (s) the pattern is discarded (ie not tested), thus the examiner takes the position that such limitations are disclosed by the combination of Freeman and D1.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENAN CEHIC whose telephone number is (571)270-3120. The examiner can normally be reached on Monday through Friday 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KWANG BIN YAO can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenan Cehic/
Examiner, Art Unit 2416

/Kwang B. Yao/
Supervisory Patent Examiner, Art Unit 2416